19.4 A Single-Chip Dual-Band CDMA2000 Transceiver in 0.13µm CMOS

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Keeping pace with the steady advances in the development of even finer gate length technologies, BiCMOS as the formerly preferred process for radio-frequency design [1,2] has increasingly been replaced by standard CMOS technologies that enable the integration of complex digital circuitry on the same die at reasonable costs in terms of required area and power consumption.

A single-chip dual-band CDMA2000 transceiver comprising a zero-IF receiver and an I/Q direct-conversion transmitter is presented. In addition to all required analog building blocks for reception and transmission in the North-American cellular and PCS bands (Band Class 0 and 1), the chip features two fully integrated synthesizers including VCOs for RX and TX (Fig. 19.4.1) for minimum external component count.

Principal challenges in CDMA2000 receiver design arise from the 900kHz AMPS-blocker in three ways: firstly, cross-modulation into the band of interest with the TX-leakage; secondly, reciprocal mixing of the VCO phase noise; and thirdly, third-order intermodulation with a blocker at a frequency offset of 1.7MHz. Since all three effects appear in the RF domain, filtering of the closely spaced interfering signals is not an option due to inadequate selectivity. Thus, sufficient attenuation of the TX leakage into the receive path by the duplexer and by a SAW band-select filter after the external LNA with 14dB gain, 1.7dB NF, and 8.3dBm IIP3 (Fig. 19.4.1) is required. In addition, proper linearity while exhibiting low noise is a key design goal for all implemented building blocks.

The input to the integrated RX front-end is formed by a self-matched highly linear common-gate LNA for each band with an NF = 4.5dB and IIP3 = 9.3dBm at a gain of 11dB drawing 3.9mA. At its output the two bands are combined to a lean single path allowing for flexibility and area saving at the cost of higher parasitic capacitance at the mixer input and in the LO chain. In the latter one, a new current-domain concept realized by a transconductance amplifier located close to the synthesizer and a low-ohmic input to a programmable prescaler avoids multiple LO interconnects and limits degradation due to the parasitic capacitances (Fig. 19.4.2).

The LO signal is generated by a type-II ΔΣ fractional-N PLL with partly integrated loop filter. The dynamic loop design is done with respect to low phase noise at 900kHz and 1250kHz frequency offsets for the Cell/PCS bands to limit the interference due to reciprocal mixing. A programming option is to use a capacitive multiplier which replaces all external loop filter components at the cost of PLL in-band phase noise. The overall PLL noise at 900kHz and 1250kHz offset frequencies is dominated by the fully integrated 4GHz VCO showing measured performance of –132.9dBc/Hz@900kHz and –133.6dBc/Hz@1250kHz for a center frequency of 1788MHz.

For the demodulator as a main contributor to the above mentioned large-signal disturbances, its severest requirement is the IIP3 of 16dBm. Since source degeneration for linearization is excluded due to noise reasons, the required high linearity is accomplished by optimizing the dimensions and biasing the dominant input transistors in deep strong inversion. In order to avoid linearity degradation by limited voltage headroom, the Gilbert-topology uses an active load and provides a current-mode output to the succeeding 1st-order low-pass filter (Fig. 19.4.2). Thus, the signal swing at the filter output can be as high as the entire supply range. This allows for increasing the demodulator gain determined by R1, which results in decreased filter capacitor C1 and therefore lower area usage. The demodulator IIP2 specification of 62dBm is exclusively met by highly symmetric layout without utilization of calibration.

The major design objective for baseband processing is to minimize the analog signal processing by using a high-resolution ADC and performing channel filtering in the digital domain. Thus, a biquad is implemented, which together with the demodulator forms a 3rd-order butterworth filter mainly for attenuation of the 1700kHz blocker and far-off interferers. In contrast to previously published designs using higher-order filters [1, 2], this solution benefits from little sensitivity of the filter attenuation to the process variations. A 5b alignment is hence sufficient to set the corner frequency to 750kHz with an accuracy of 1%. Eventually, the described RX chain without external LNA and band-select filter achieves the typical performances summarized in Fig. 19.4.3 while drawing 61mA and 59mA in Cell and PCS modes, respectively.

Furthermore, in a test version, the ADC of [4] and the RX digital front-end (DFE) of [5] have been added to demonstrate the performance of the entire analog/digital receiver lineup. The 3rd-order 4b CT-ΔΣ ADC, whose loop filter is modified for CDMA2000 with respect to stability, out-of-band attenuation, and noise, features 650kHz bandwidth and in the presence of a 900kHz blocker a measured noise floor of –90dBFS (Fig. 19.4.4), is achieved which is sufficient for converting the received signal into the digital domain. Figure 19.4.5 exhibits a maximum output SNR of 23dB measured at the DFE output for the more critical PCS band indicating feasibility for evolution-data-optimized (EVDO)-operation with the presented receiver lineup.

On the TX side, an I/Q direct-modulation architecture is used that comprises of I/Q PGAs, I/Q baseband filters, I/Q-modulators, and output drivers for Cell and PCS band. The LO signal is provided by a fully integrated type-II fractional-N PLL with integrated VCO. For CMOS implementation, the key transmitter design challenge is to achieve maximum output power of the output driver while exhibiting good linearity at low power consumption. In order to satisfy 25dBm antenna power specified for CDMA2000 [3], for a typical PA considered in this paper, a transmitter output power of 9dBm is required. By careful circuit and layout optimization, $P_{out,max}$ is boosted to 13.5dBm while achieving ACP1=–57dBc/30kHz and ACP2=–69dBc/30kHz @9dBm with a CDG4 urban current draw of 34mA. Figure 19.4.6 shows the PCS RHO performance over a dynamic range of beyond 90dB with a TX noise in RX band equal –142dBm/Hz @ 9dBm. The degradation of RX noise figure by 0.2dB proves adequacy of the PLL and the Gilbert-type modulator. A self-alignment achieves a maximum carrier suppression of –40dB thus making factory calibration dispensable.

The chip has been fabricated in a 1P6M 0.13µm CMOS process including MIM capacitors, occupies 8.4mm², and is housed in a very very thin fine pitch semiball grid array (WFSGA-81) package. Figure 19.4.7 shows a micrograph of the die. The presented results prove that a fully-integrated single-chip transceiver for CDMA2000 is feasible and shows competitive results to multi-chip solutions.

Acknowledgement:
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[1] H. Waite, P. Ta, J. Chen, et al., "A CDMA2000 Zero-IF Receiver With Low-Leakage Integrated Front-End," *J. Solid State Circuits,* vol. 39, pp 1175-1179, Jul., 2004.
[2] V. Aparin, N. Kim; G. Brown, et al., "A Fully-Integrated Highly Linear Zero-IF CMOS Cellular CDMA Receiver," *ISSCC Dig. Tech.. Papers,* pp. 324-325, Feb., 2005.
[3] CDMA2000 standard 3GPP2 C.S0011-B.
[4] L. Dörrer, F. Kuttner, P. Greco, and S. Derksen, "A 3mW 74dB SNR 2MHz CT ΣΔ ADC with a Tracking-ADC-Quantizer in 0.13µm CMOS," *ISSCC Dig. Tech. Papers*, pp. 492-493, Feb., 2005.
[5] G. Hueber, G. Strasser, R. Stuhlberger et al., "A Digital-Front-End for Multi-Mode/Multi-System Capable Receivers for Cellular Terminals," *IEEE Vehicular Technology Conference*, Sept., 2006.

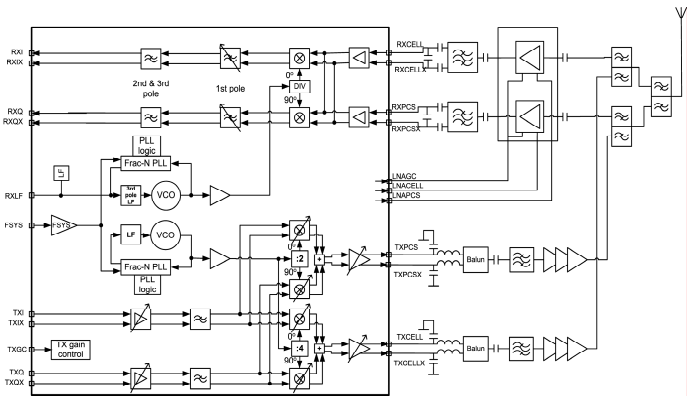

Figure 19.4.1: Transceiver block diagram including application circuitry.

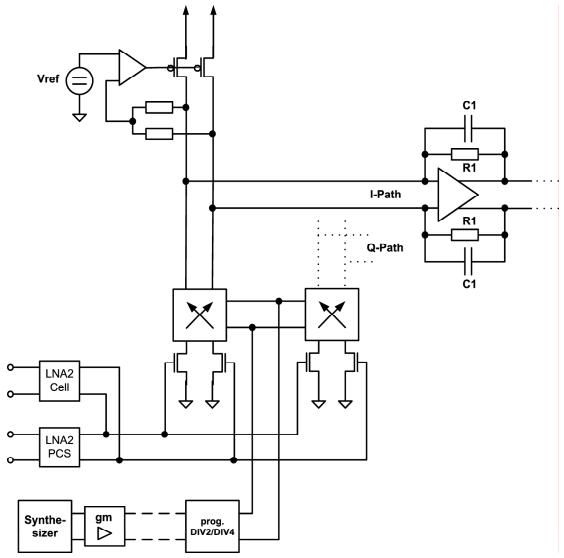

Figure 19.4.2: Demodulator with its interface to baseband.

	Cell	PCS
Technology	0.13µm CMOS	
Area	8.4mm²	
Supply Voltage	1.5V/2.5V	
Receiver		
Gain [dB]	33.2	32
Noise Figure [dBm]	8.7	9.2
IIP3 [dBm]	2	0.5
IIP2 [dBm]	51	50.8
RX-path Current [mA]	61	59
max. PCS Output SNR (incl. DFE) [dB]	25	23
Transmitter		
$P_{out,max}$ [dBm]	12.3	13.5
ACPR1/ACPR2 [dBc/30kHz]	−59/−72	−57/−69
RHO @9dBm	0.998	0.995
TX noise in RX [dBm]	−142	−142
CDG4 urban current [mA]	39	34

Figure 19.4.3: Performance summary.

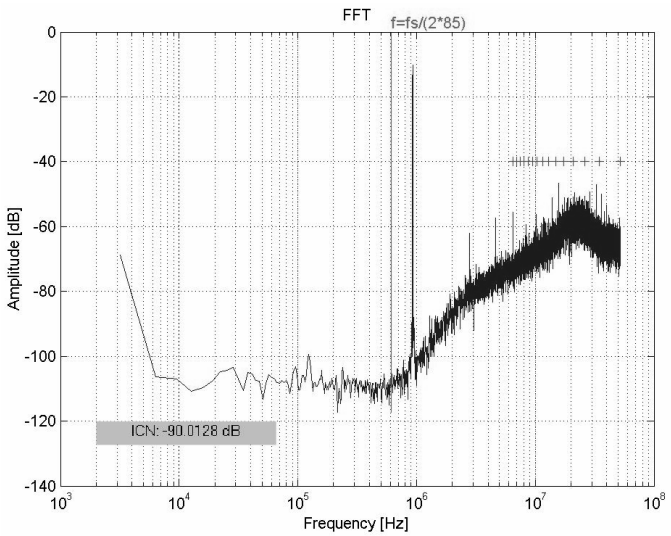

Figure 19.4.4: Test version ADC with 900kHz blocker.

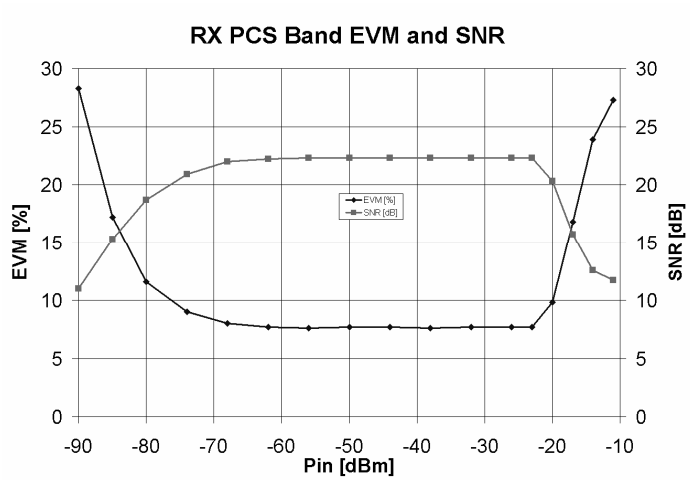

Figure 19.4.5: SNR and EVM versus P_{in} for the entire RX chain.

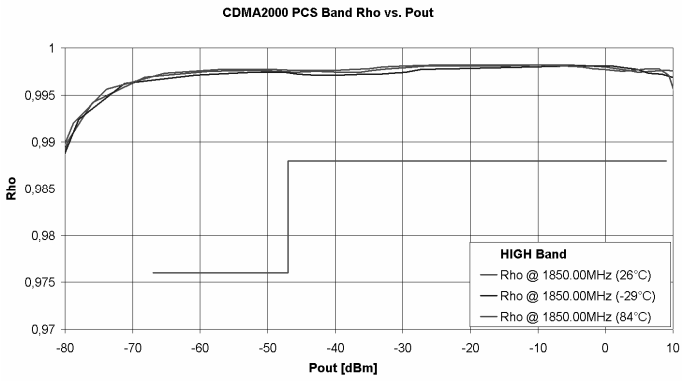

Figure 19.4.6: TX Rho versus P_{out} for PCS band.

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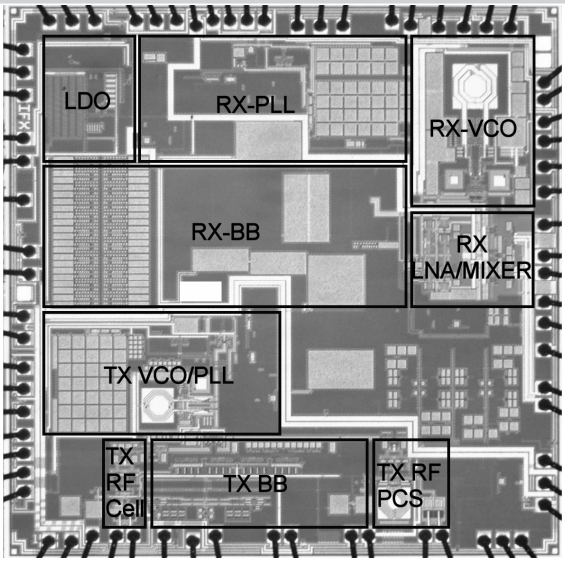

Figure 19.4.7: Chip micrograph.

